AMENDMENTS TO THE CLAIMS

1-54. (Canceled)

55. (Currently amended) A method of processing an implanted region, comprising:

forming at least one transistor gate over a substrate of a first conductivity type;

forming an implanted well region of said first conductivity type below at least a portion of said transistor gate, said implanted well region being formed to a thickness of about 4,000 to about 40,000 Angstroms; and

providing an electrical device laterally displaced from said implanted region.

56. (Canceled)

57. (Original) The method of claim 55, wherein said implanted well region is formed below about half the channel length of said transistor gate.

58. (Original) The method of claim 55, wherein said implanted well region is formed by conducting an implant with dopants of said first conductivity type in an area of said substrate below half the channel length of said transistor gate.

59. (Original) The method of claim 55, wherein said implanted well region has an implant dose of about 5×10^{11} to about 5×10^{13} atoms per cm^2.

60. (Original) The method of claim 55, wherein said electrical device is an imager.

61. (Original) The method of claim 60, wherein said electrical device is a CMOS imager.

62. (Original) The method of claim 60, wherein said electrical device is a CCD imager.

63. (Original) The method of claim 60, wherein said electrical device is a photosensor, a photodiode, a photoconductor or a photogate.

64. (Original) A method of forming a photodiode for a pixel sensor cell, comprising:

forming at least one isolation region in a substrate;

forming a gate stack over said substrate;

forming an implanted well region of a first conductivity type in said substrate and adjacent at least a portion of said isolation region and of said gate stack;

forming a doped region of a second conductivity type in said substrate and laterally displaced from said implanted well

region; and

forming a doped layer of said first conductivity type in said substrate, said doped layer being in contact with said doped region of said second conductivity type.

65. (Original) The method of claim 64, wherein said implanted well region is formed below at least a portion of said isolation region.

66. (Original) The method of claim 64, wherein said implanted well region is formed below about half the channel length of said gate stack.

67. (Original) The method of claim 64, wherein said doped region of said second conductivity type is laterally displaced from said implanted well region by about 1,000 Angstroms to about 5,000 Angstroms.

68. (Original) The method of claim 67, wherein said doped region of said second conductivity type is laterally displaced from said implanted well region by about 1,000 Angstroms to about 3,000 Angstroms.

69. (Original) The method of claim 64, wherein said implanted well region is implanted with a p-type dopant and an implant dose of about 5×10^{11} to about 5×10^{13} atoms per cm^2.

70. (Original) The method of claim 64, wherein said implanted well region is formed to a thickness of about 4,000 to about 40,000 Angstroms.

71. (Original) The method of claim 64, wherein said implanted well region is formed subsequent to the formation of said gate stack.

72. (Original) The method of claim 64, wherein said implanted well region is formed prior to the formation of said gate stack.

73. (Original) The method of claim 64, wherein said gate stack is part of a transfer transistor.

74. (Original) The method of claim 64, wherein said gate stack is part of a reset transistor.

75. (Original) The method of claim 64, wherein said photodiode is a p-n photodiode or an n-p photodiode.

76. (Original) The method of claim 64, wherein said photodiode is part of a CCD sensor.

77. (Original) The method of claim 64, wherein said photodiode is part of a CMOS sensor.

78. (Original) A method of forming a p-n photodiode for a CMOS imaging device, said method comprising:

forming at least one trench isolation region in a silicon substrate;

forming a gate stack of a transistor over said silicon substrate;

and

forming a doped well region below about half the channel length of said gate stack and below said trench isolation region by implanting p-type ions in said silicon substrate, said doped region having an implant dose of about 5×10^{11} to about 5×10^{13} atoms per cm^2.

79. (Original) The method of claim 78 further comprising the steps of:

forming an n-type doped region in said silicon substrate; and

forming a p-type doped layer in said silicon substrate and above said n-type doped region, said p-type doped layer and said n-type doped region being laterally displaced from said doped well region.

80. (Original) The method of claim 79, wherein said n-type doped region is laterally displaced from said doped well region by about half the channel length of said gate stack.

81. (Original) The method of claim 78, wherein said doped well region is formed below about half the channel length of said gate stack.

82. (Original) The method of claim 78, wherein said doped well region is formed to a thickness of about 4,000 to about 40,000 Angstroms.